	Type	L #	Hits	Search Text
1	BRS	L1	322665	((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.
2	BRS	L2	330	1 and (skip$ near7 (process$3 or step$1 or judgement))
3	BRS	L3	23	1 and (skip$ near7 (process$3 or step$1 or judgement))
4	BRS	L4	307	1 and (skip$ near7 (process$3 or step$1 or judgement))
5	BRS	L5	18	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and (skip$ near7 (process$3 or step$1) near7 (judg$5 or determin$3))
6	BRS	L6	0	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and (skip$ near7 (process$3 or step$1) near7 (judg$5 or determin$3))
7	BRS	L7	322828	((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.
8	BRS	L8	18	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and (skip$ near7 (process$3 or step$1) near7 (judg$5 or determin$3))

	DBs	Time Stamp	Comments	Error Definitio	Errors
1	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/08 15:18			0
2	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/09/08 15:20			0
3	EPO; JPO; DERWENT	2004/09/08 15:21			0
4	USPAT; US-PGPUB	2004/09/08 15:21			0
5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:22			0
6	EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:23			0
7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:24			0
8	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:24			0

	Type	L #	Hits	Search Text
9	BRS	L9	8	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and ((bypass$3 or (by adj pass$3)) near7 (process$3 or step$1) near7 (judg$5 or determin$3))
10	BRS	L10	10	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and ((omit$5 or omission) near7 (process$3 or step$1) near7 (judg$5 or determin$3))
11	BRS	L11	47	(((semiconductor or wafer$1 or chip$1 or (integrated adj circuit$3) or ic$2) near7 (fab$8 or manufactur$3 or processing)).ti,ab.) and ((eliminat$4) near7 (process$3 or step$1) near7 (judg$5 or determin$3))

	DBs	Time Stamp	Comments	Error Definitio	Errors
9	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:25			0
10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:26			0
11	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/08 15:26			0